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ADP012153

TITLE: Electrical Property of Vertically Grown Carbon Nanotube and Its Application to the Nanofunctional Devices

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TITLE: Materials Research Society Symposium Proceedings. Volume 675. Nanotubes, Fullerenes, Nanostructured and Disordered Carbon. Symposium Held April 17-20, 2001, San Francisco, California, U.S.A.

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ADP012133 thru ADP012173

Mat. Res. Soc. Symp. Proc. Vol. 675 © 2001 Materials Research Society

Electrical Property of Vertically Grown Carbon Nanotube and Its Application to the Nanofunctional Devices

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ABSTRACT

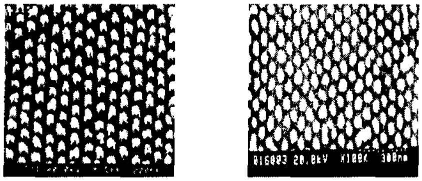
A highly ordered porous alumina array which hole size is decreased down to 20nm was fabricated by a two step anodization method. Carbon Nanotube was grown vertically with thermal CVD at 600~700℃. By using rapid thermal annealing method, low-ohmic contact was formed between multi wall nanotubes and metal electrode and its resistance shows tens to hundreds Ω. The alumina layer which is existed between nanotube and electrode acts as a barrier for conductance. The resistance of carbon nanotube shows the temperature(T^{-1}) dependence at 4.21K < T < 19.9K and semiconducting behavior at this temperature region.

INTRODUCTION

The 10 years of carbon nanotube (CNT) since the discovery of 1991[1] have been a marvelous period for CNT itself and scientists studying the various properties of CNT. The electrical property, especially, can be varied from semiconducting to metallic according to the CNT's diameter, chirallity and doping status.[2-4] Multi wall nanotube(MWNT) has a complicate structure rather than single wall nanotube(swnt) having a ideal one dimensional wire structure but has a merit to the easiness of synthesis and purification. The research for device using mwnt has been studied by many but the difficulties of reproducible high quality nanotube-control and selective nano-positioning to device tool remain as a barrier for advanced device. In order to overcome these barriers, CNT is grown selectively in anodic aluminum oxide(AAO) template[5] and is characterized electrical transport property. The feasibility of selectively grown CNT to the nano-functional device has been investigated

EXPERIMENTAL

Carbon nanotube arrays have been fabricated on porous anodic aluminum oxide (AAO) which is controlled by conventional anodization method.[5] High purity aluminum sheet (99.999%) was used as a substrate and highly ordered nano-pore was



a) b)

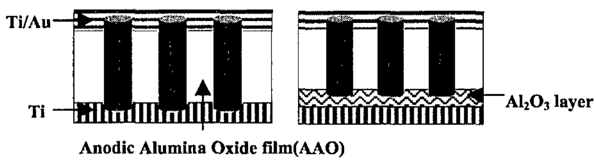
Figure 1. SEM images of carbon nanotube in porous alumina and schematic : (a) Top surface of 20nm nanotube after removing graphite layer. (b) the back side of nanotube on AAO after etching away the aluminum oxide with ion milling.

fabricated by anodization technique. Hole diameter is 20nm and fabricated by using sulfuric acid as a anodizing solution. Carbon nanotube was synthesized in the pores by thermal CVD at the temperature range of 600~700°C without catalyst. Figure 1 is scanning electron microscopy(SEM) images showing a both(top, bottom) view of the nanotube after etching the AAO template by ion milling. We carried out two probe conductance measurement of nanotube on AAO followed by metal electrode deposition in this experiment. Figure 2 shows the schematic of metal deposited test sample. The metal electrode is Au/Ti and the electrode shape is a circular type with the hole size of 70㎛. The estimated number of holes in one circular electrode is around 6×10^6. The Ti was directly deposited on oxide face(bottom) of sample and Au/Ti was deposited on the top surface where graphite was removed. In this work, two types of test sample were prepared for measurement : one has aluminum oxide barrier layer at the bottom and the other has not. It is considered that the alumina layer influences conductance on each sample because the layer acts as a tunnel junction separating the nanotubes from metal electrode.

RESULTS AND DISCUSSION

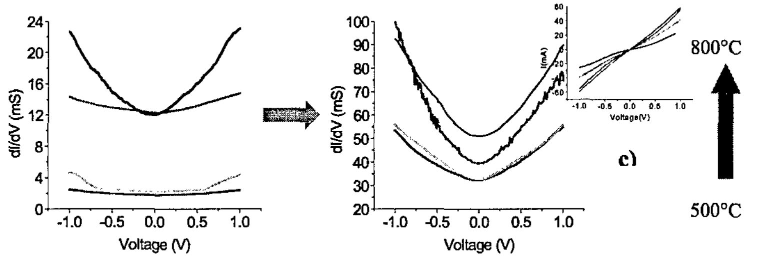
I-V characterization of nanotube is shown in Figure 3 and 4. Figure 3 shows the IV measurement that was performed under the vacuum after rapid thermal annealing(RTA) at the range of 500~800°C. In case of Figure 3(a), the conductance(dI/dV) of sample having oxide layer is 1.77mS at 500°C RTA and increased 12mS at 800°C. This means that RTA plays a important role in increasing conductance by reducing contact resistance between metal electrode and nanotube. Sample (b) doesn't have an oxide layer and shows higher conductance than that of

Sample	Diameter	Surface condition
a	20nm	No Al_2O_3
b	20nm	Al_2O_3



a) b)

Figure 2. Table of sample types and schematic of test sample.



a) b)

Figure 3. The conductance(dI/dV) change of nanotube due to the RTA. a) oxide layer sample b) no oxide layer sample. It shows that increased conductance value is due to the RTA and oxide barrier. c) The IV data of sample which is exposed at both side. It shows that higher current flow is increased as annealing temperature is increased

sample (a). The conductance difference is almost four times increment(50mS) when compared conductance at zero bias voltage. Zhang *et al* reported that the carbide layer begins to form at the carbon nanotube and Ti interface after above temperature(> 800°C).[6] They showed that the formation of a carbide layer is caused by the surface diffusion of metal atoms to the interface and the diffusion rate is very slow. The nanotube-carbide bulk hetero structures is made through metal atoms transfer into the nanotube by annealing for 20min and forms bulk junctions.[6] In our experiment the annealing time is relatively short (30sec) compared to the Zhang *et al*'s work and it could prevent forming bulk hetero-junctions. Therefore the short, low and rapid temperature annealing process enabled to make a better nanotube-metal(Ti) contact for electrical measurements. Figure 3(c) shows conductance comparison of sample (b) due to the RTA. The more increased annealing temperature, the conductance increased upto 60mA. Assuming the resistance of the contact and the nanotube to be R_c and R_{nt}, the total resistance(R_t) of sample (b) is given by $R_t = 2R_c + R_{nt}$ (R_c is the resistance between Ti and nanotube at both side) while the total resistance of sample (a) is $R_{ta} = R_c + R_{oxide} + R_{nt}$. To get resistance of nanotube itself, it needs to be removed oxide layer because investigating the total resistance of (a) sample is very complicated and cannot be explained clearly. Recently, Davydov et al. reported that the resistance of individual 48nm nanotube would be $\sim 6 \times 10^6 \Omega$ assuming a similar resistivity to carbon film ($\rho = 3 \sim 5 \times 10^{-2} \Omega$.[7] Because nanotube sample with a surface contact area of 70㎛ contains approximately $\sim 10^6$ tubes, an estimated resistance of nanotube array is 6Ω. In our work, we intended to get the resistance of nanotube only through reducing contact resistance(R_c) by RTA process. As the result of that process, resistance is decreased to 20Ω. This experimentally measured value is 1 order higher than the estimated resistance. This shows significantly lower value than that of previously reported work by other group. It implies that metal electrode using Ti/Au shows better contact between nanotube and electrode and RTA process is an effective tool for reducing contact resistance. The electric characteristics at low temperature is shown in Figure 4. In case of sample (a), the shape of conductance exhibit zero-bias cusps of the form $dI/dV \approx V^{\alpha}$ where α is in the range 0.45~0.10 for $4.21 < T < 9.99K$ and zero-bias conductance shows T^{-1} dependence in the temperature range $4.21 < T < 19.99K$

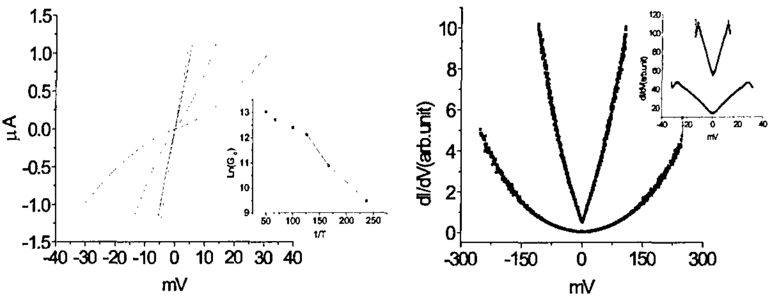


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Figure 4. a) IV measurement at low temperature and inset shows temperature dependence of Ln G_o. Conductance suppressed near V=0 for T < 7.9K and ohmic behavior was shown at temperature(> 7.9K). (b) dI/dV comparison data(4.2, 6.1K) due to the oxide layer sample. Oxide layer having sample shows the coulomb blockade at 4.2K temperature

in the right inset of Figure 4(a). Through $G_o \sim \exp(AT^{-1})$, activation energy(E) is 2~3meV and shows the semiconducting behavior at this temperature region. Two types of conductance pattern are exhibited in Figure 4(b). Anomaly zero-bias G_o that means oxide layer between nanotube and electrode plays a key role for current blockade. In the inset of Figure 4(a), nanotube sample which doesn't have oxide layer shows normal zero-bias conductance while conductance suppressed near V=0 at lower temperature(< 7.9K). J. Haruyama *et al* reported that nanotube sample having 5nm oxide layer shows zero-bias G_o varied near T=5K and the shape at 2K is quite different form shown as a reference 8 and also reported that it is evident that the nanomaterials connected to the single tunnel junctions strongly contribute to the G_o anomaly.[4] In our work, zero-bias G_o variation shows almost same pattern compared with J. Haruyama et al's work while oxide barrier layer between nanotube and metal electrode is almost 20nm. The shape of zero-bias G_o varied near T=6.01K and the shape at 4.21K is different from the data in right inset of Figure 4(b) although the thickness of oxide layer is bigger than that of J. Haruyama et al's sample. The contact area of metal electrode is a dot shape with 70㎛ diameter and it includes around 10^6 nanotubes. Each nanotube acts as a electron transfer tunnel and oxide layer acts also as a single tunnel junction. However, Such structure including many nanotubes in a dot-shape electrode can be regard as a kind of mass systematically so oxide layer between nanotube and metal can be also regard as a kind of multi-tunnel junction. Assuming all nanotubes in the electrode act as a pathway to electric current, electrons tranfer across the oxide layer easily at the temperature(> 7.9K) through carbon nanotube and coulomb blockade behavior was disappeared above same temperature region.

CONCLUSION

Highly vertically ordered anodic alumina oxide(AAO) template was fabricated by anodization method and carbon nanotube was synthesized at 600~700°C by thermal

CVD. The rapid thermal annealing process made ohmic contacts between Ti-Au electrode and carbon nanotube. The aluminum oxide layer acts as a barrier for conductance and nanotube having oxide layer shows coulomb blockade at lower temperature(< 4.21K). Carbon nanotube shows the temperature(T^{-1}) dependent at 4.21K < T < 19.9K and semiconducting behavior at this temperature region.

ACKNOWLEDGEMENTS

This work was supported by The National Program for Tera-Level Nanodevices of the Ministry of Science and Technology as one of The 21 Century Frontier Programs.

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